AMENDMENTS TO THE CLAIMS

The following is a complete listing of the claims indicating the current status of each claim and including amendments currently entered as highlighted.

1-39 (canceled)

40. (currently amended) A method for providing a digital output signal representing at least one analog input signal, comprising:

(a) feeding an analog circuit with said at least one analog input signal and a plurality of discrete correction signals;

(b) said analog circuit providing analog monitoring outputs,

wherein said at least one analog input signal and said discrete correction signals are jointly related by a relationship to said analog monitoring outputs, said relationship ~~by a model~~ having an identification algorithm;

(c) receiving said analog monitoring outputs and a synchronization clock and implementing a negative feedback control loop by said feeding said analog circuit with said discrete correction signals, in order to keep at least one of said analog monitoring outputs to be within a previously defined constraint;

(d) identifying said relationship thereby ~~said model, by~~ creating an internal representation of said relationship;

(e) calculating said digital output signal by using a digital representation of said discrete correction signals and said internal representation, wherein said digital output signal represents said at least one analog input signal.

41. (previously presented) The method of claim 40, further comprising the step of, prior to said (a) feeding:

(f) training by inputting a plurality of known analog training signals into said analog circuit.

42. (previously presented) The method of claim 40, wherein said analog circuit is time varying according to said synchronization clock.

43. (previously presented) The method of claim 40, wherein said discrete correction signals are based on selectably either at least two previously defined values or at least two previously defined waveforms.

44. (currently amended) The method of claim ~~1~~40, wherein said analog circuit is a linear analog circuit.

45. (previously added) The method of claim 44 wherein said identifying includes a least- mean square (LMS) technique.

46. (previously added) The method of claim 40, wherein said calculating is only up to a previously defined partial reconstruction of said at least one analog input signal.

47. (previously added) The method of claim 40, wherein said identifying is repeated occasionally within a training period, and said identifying includes feeding at least one analog training signal during said training period.

48 (previously added) The method of claim 47, wherein said at least one analog signal is produced by feeding known digital signals to a digital to analog converter, said known digital signals driving said at least one analog training signal.

49. (previously added) The method of claim 47, where said identifying is performed in the background by interleaving said at least one analog input signal and said at least one analog training signal.

50. (previously added) The method of claim 40, wherein said identifying uses available statistical information about said at least one analog input signal.

51. (currently amended) The method of claim 47, wherein said at least one analog training signal is produced by cascading said analog circuit with at least one additional analog circuit fed by a known reference signal and said identifying is of a ~~joint model~~relationship between said known reference signal and an output of said analog circuit, ~~and said at least one additional analog circuit.~~

52. (currently amended) ~~A method providing a digital output signal representing at least one analog input signal by~~ The method of claim 40, wherein said analog circuit is a multi-stage ~~system~~ analog circuit including a plurality of stages, ~~each stage including an analog circuit~~, the method further comprising the steps of:

(a) ~~providing~~ for each said stage, except the first stage, ~~the analog circuit~~ receiving as input signals at least one analog signal from a preceding stage and at least one discrete correction signal;

(b) ~~the analog circuit of~~ the first stage receiving as inputs at least one discrete correction signal and at least one analog input signal;

(c) for each said stage, ~~the analog circuit~~ providing at least one analog monitoring output,

(d) providing, for each stage of ~~said~~the multi-stage ~~system~~analog circuit, said at least one discrete correction signal,~~ by using information from other stages said information including at least one analog monitoring output, and by further using a synchronization clock, wherein said at least one discrete correction signal performs a negative feedback control loop in order to control said at least one analog monitoring output;~~

~~(e) receiving and storing from each said stage, a digital representation of said at least one discrete correction signal;and~~

~~(f) identifying a multi-stage system model~~relationship between said inputs and the at least one analog monitoring outputs of said multi-stage system, ~~by identifying a plurality of unknown parameters within said multi-stage system model, thereby creating an internal representation of a relationship~~relating between a digital representation of the discrete correction signals of all stages of said multi-stage system, to the at least one analog input signal of said multi-stage system;

~~(g) reconstructing the digital output signal using said digital representation, and said multi-stage system model, wherein the digital output signal represents the at least one analog input signal of said multi-stage system.~~

53. (previously added) The method of claim 52, wherein operation of each stage is dependent on at least one other stage.

54. (currently amended) A multi-stage analog signals sampler, wherein each stage of the multi-stage analog signals sampler includes:

(a) an amplifier which amplifies an input analog signal, thereby producing an amplified analog signal;

(b) a ~~mechanism~~capacitor which at least approximately integrates said amplified analog signal, thereby producing an integrated signal;

~~(e)~~ wherein a discharge mechanism discharges ~~which causes decaying of~~ said ~~integrated~~ capacitor~~signal~~; and

(~~cd~~) a mechanism which performs a comparison of said integrated signal with at least one threshold, and adds at least one previously defined correction to said amplified analog signal, and registers an output of said comparison in a digital logic.

55. (previously added) A multi-stage analog signals sampler, wherein each stage of said multi-stage analog signals sampler includes:

(a) an amplifier amplifying an analog input signal, thereby producing an amplified analog signal;

(b) a mechanism which renders said amplifier dependent on a synchronization clock;

(c) a circuit which features a time constant on the order of a period of said synchronization clock, wherein said circuit modifies said amplified analog signal;

(d) a mechanism which provides, at least one discrete correction signal to said analog input signal, by using information from at least one other said stage, wherein said at least one discrete correction signal performs a negative feedback control loop which controls said analog input signal; and

(e) a mechanism which receives and stores, a digital representation of said at least one discrete correction signal.

56. (currently amended) The multi-stage analog signals sampler, according to claim 55, further comprising

(f) a mechanism which identifies a ~~model~~relationship between said at least one discrete correction signal, said analog input signal and said information used in said negative feedback control loop of said multi-stage analog signals sampler,

(g) a digital signal processing mechanism which calculates a digital output signal representing said analog input signal.

57. (currently amended) A parallel analog signals sampler, comprising a plurality of the multi-stage analog signals samplers according to claim 55, wherein the respective digital representations of the multi-stage signal samplers are output to a common digital signal processing mechanism, the parallel analog signals sampler

comprising a mechanism which identifies a joint ~~model~~relationship between a parallel input and the parallel output of said multi-stage analog signals samplers.

58. (previously added) The parallel multi-stage analog signals sampler, according to claim 57, wherein said mult-stage analog signals samplers are placed in close proximity, wherein crosstalk between said parallel analog signal samplers is included in said joint model.

59. (previously added) The method of claim 40, wherein at least one of said analog monitoring outputs is time continuous.

60. (canceled)